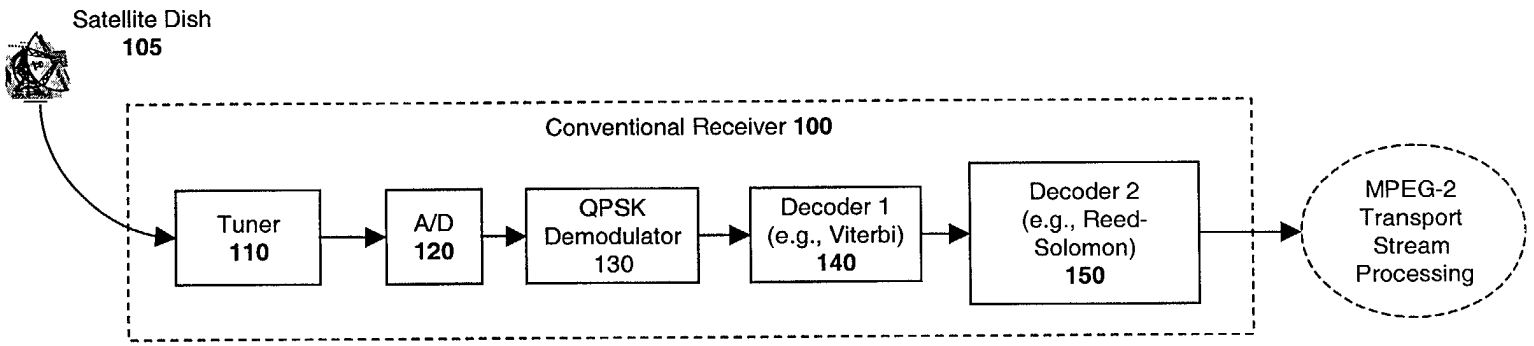

Fig. 1
Prior art

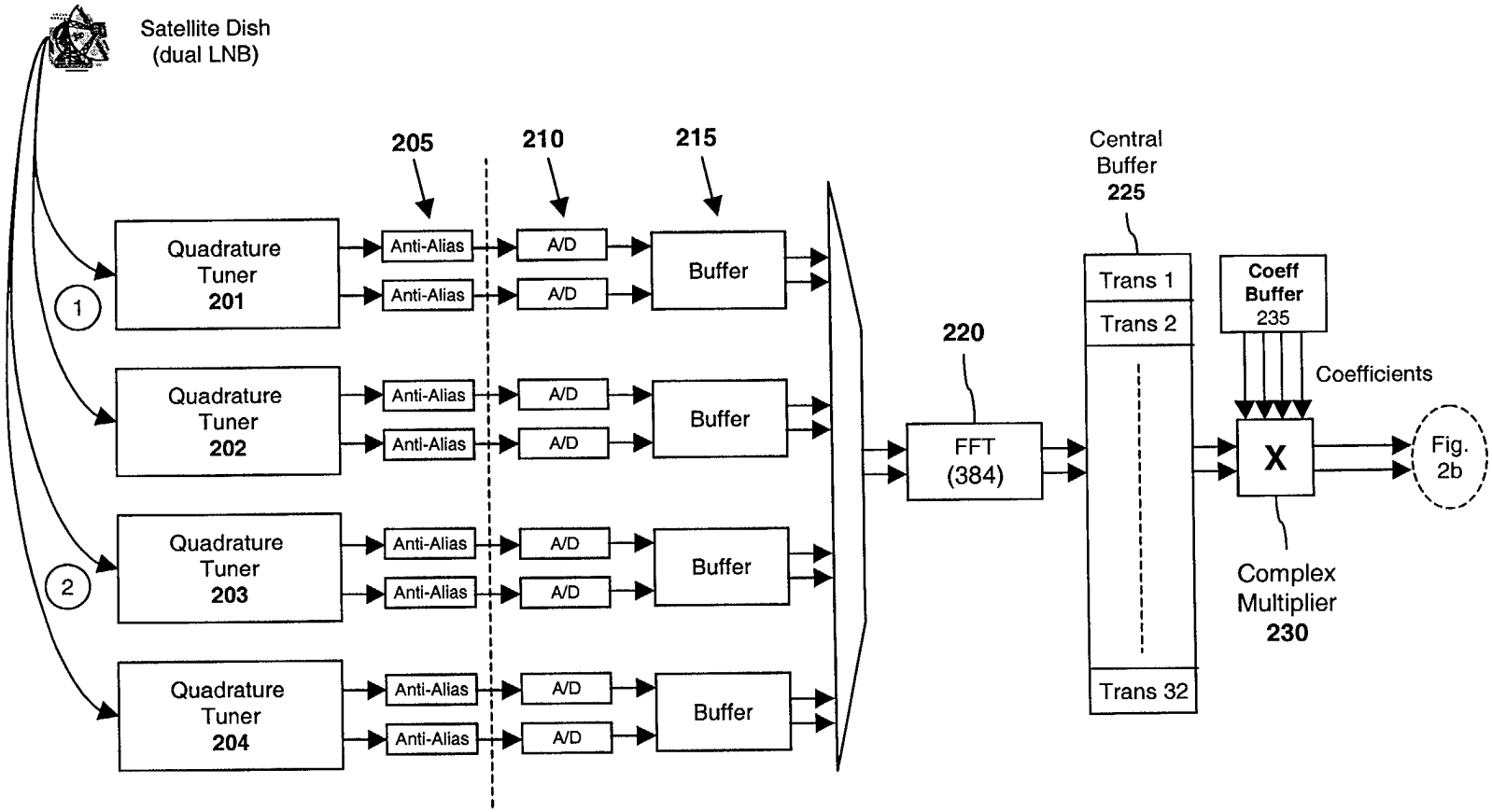

Fig. 2a

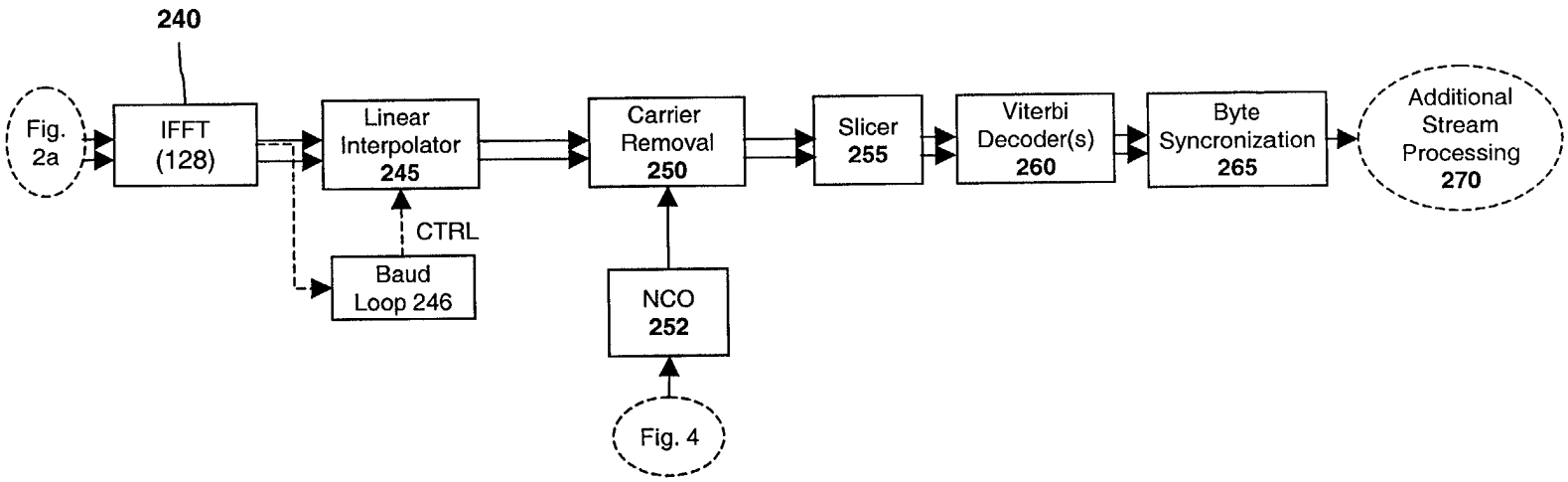

Fig. 2b

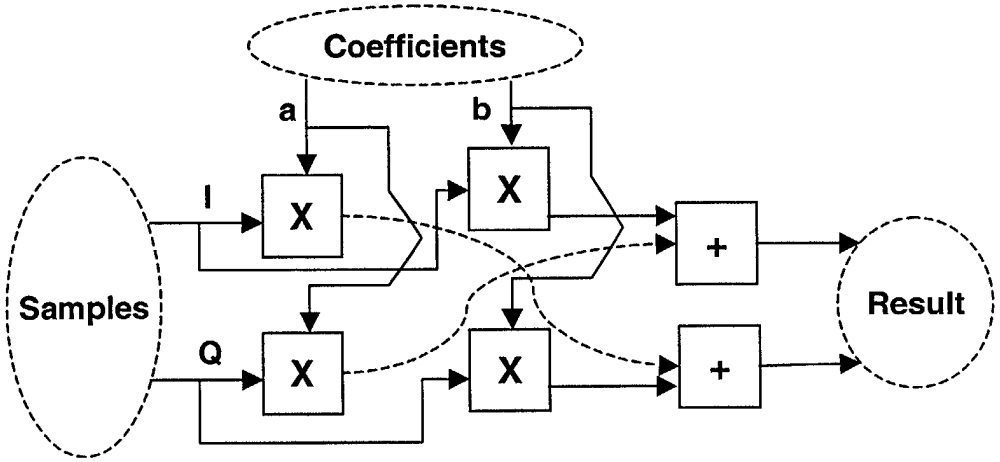

Fig. 3a

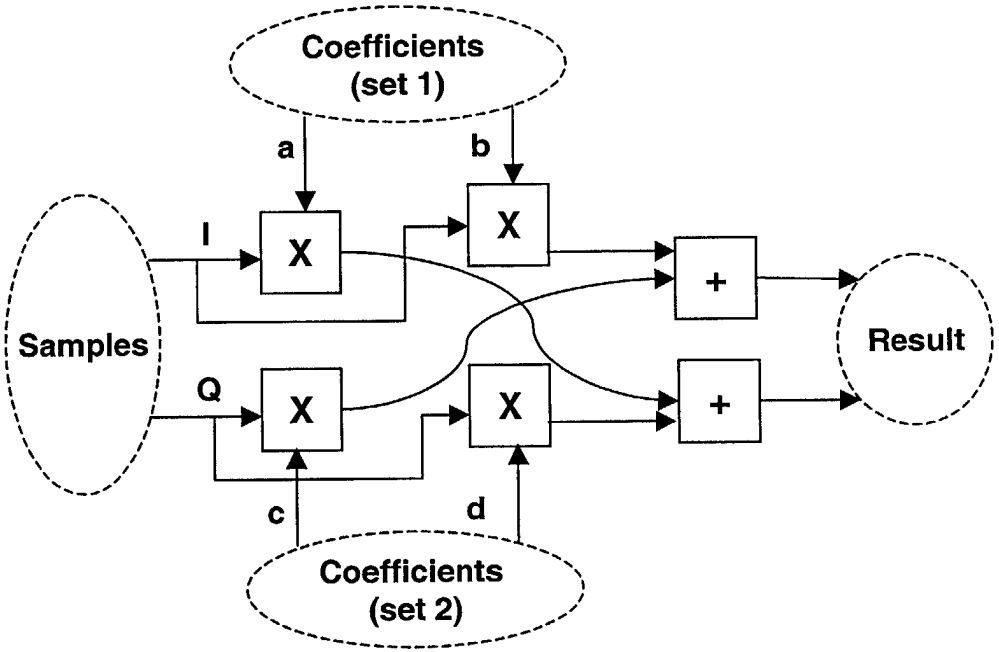

Fig. 3b

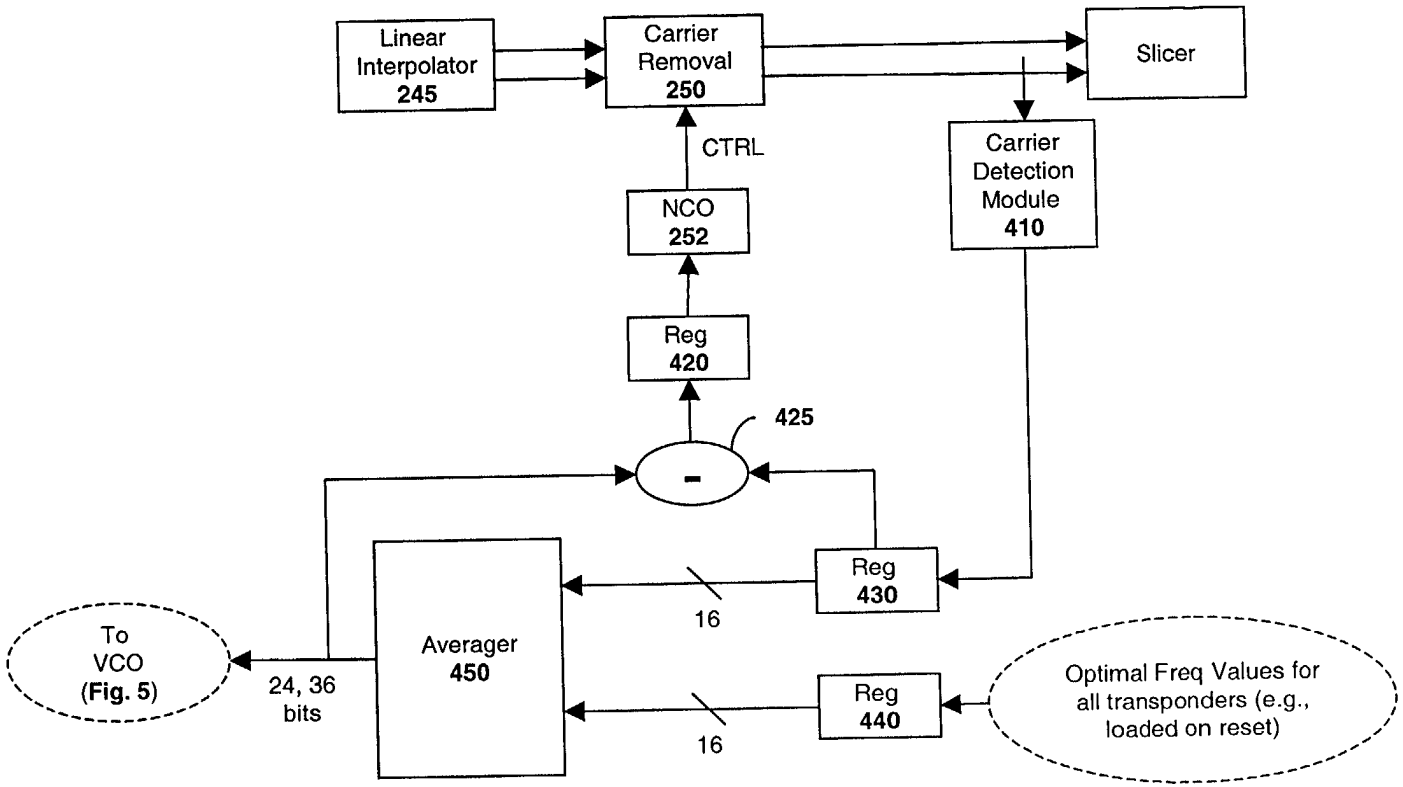

Fig. 4

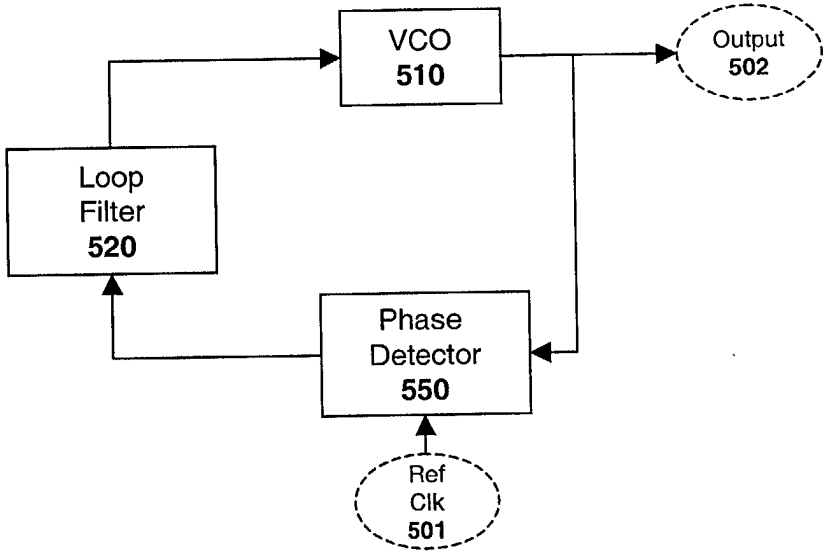
VCO
510
Output
502
Loop
Filter
520
Phase
Detector
550
Ref
Clk
501

Fig. 5a

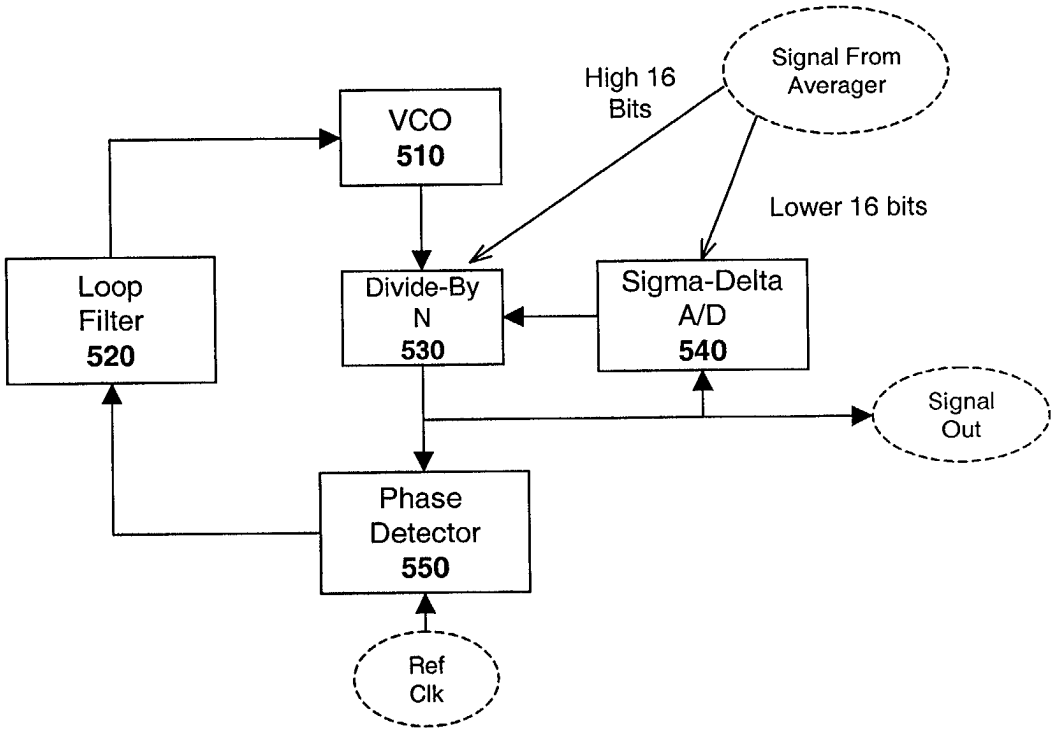

Fig. 5b

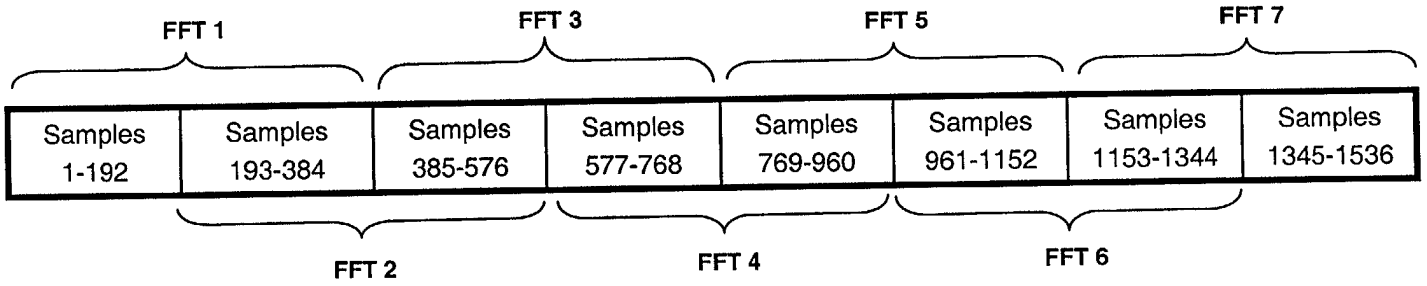

Fig. 6

FFT Input Data

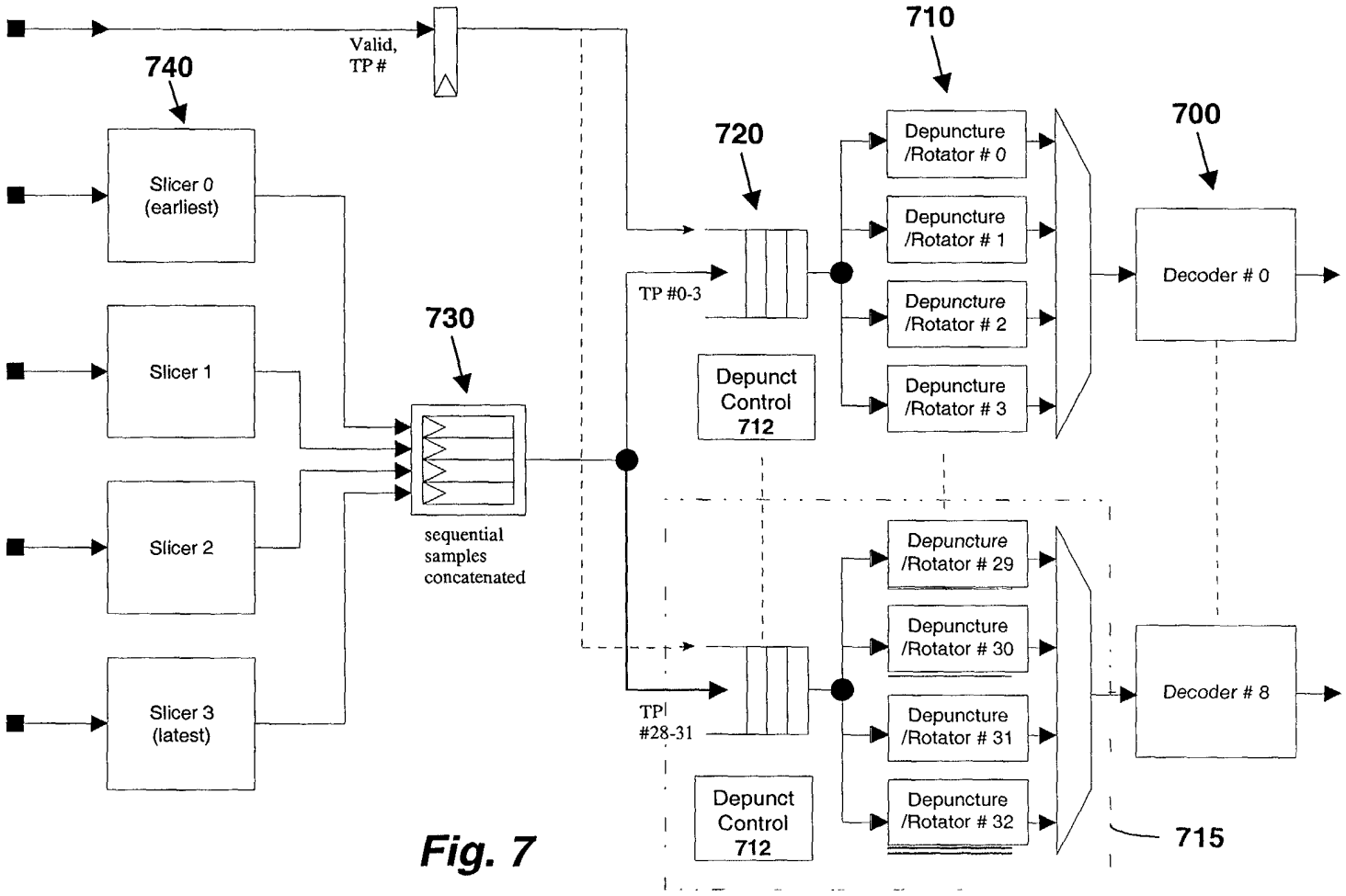

Fig. 7

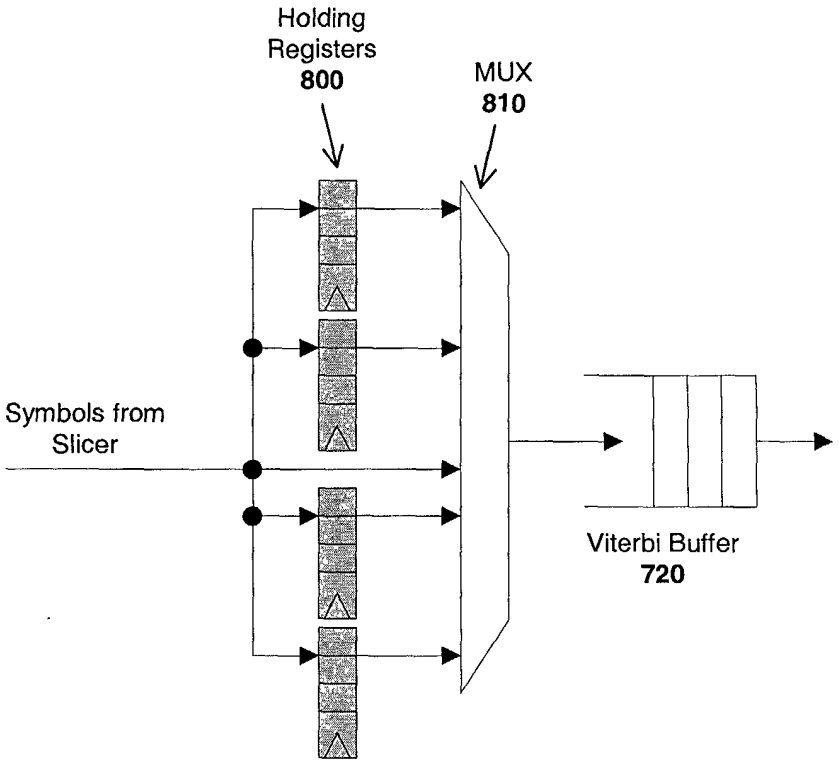

Fig. 8

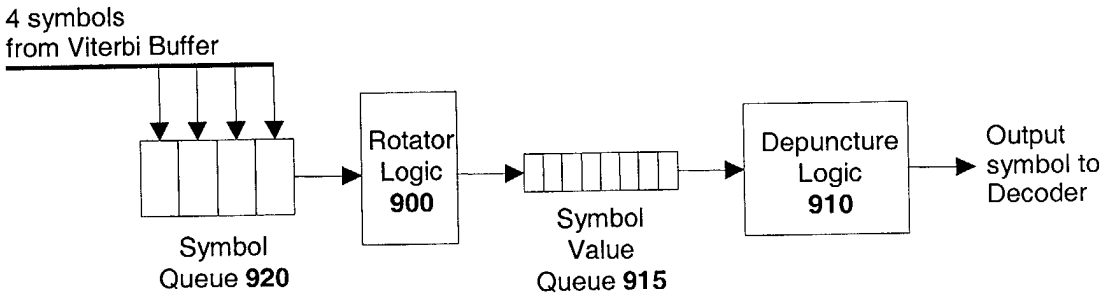

Fig. 9

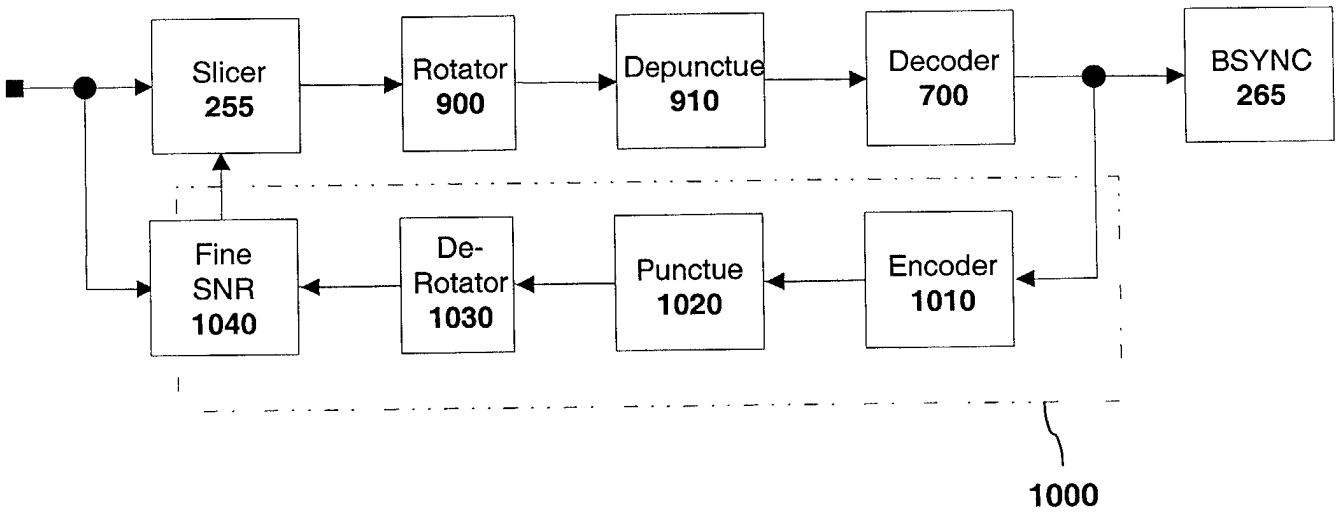
Slicer
255
Rotator
900
Depunctue
910
Decoder
700
BSYNC
265
Fine
SNR
1040
De-
Rotator
1030
Punctue
1020
Encoder
1010
1000

Fig. 10

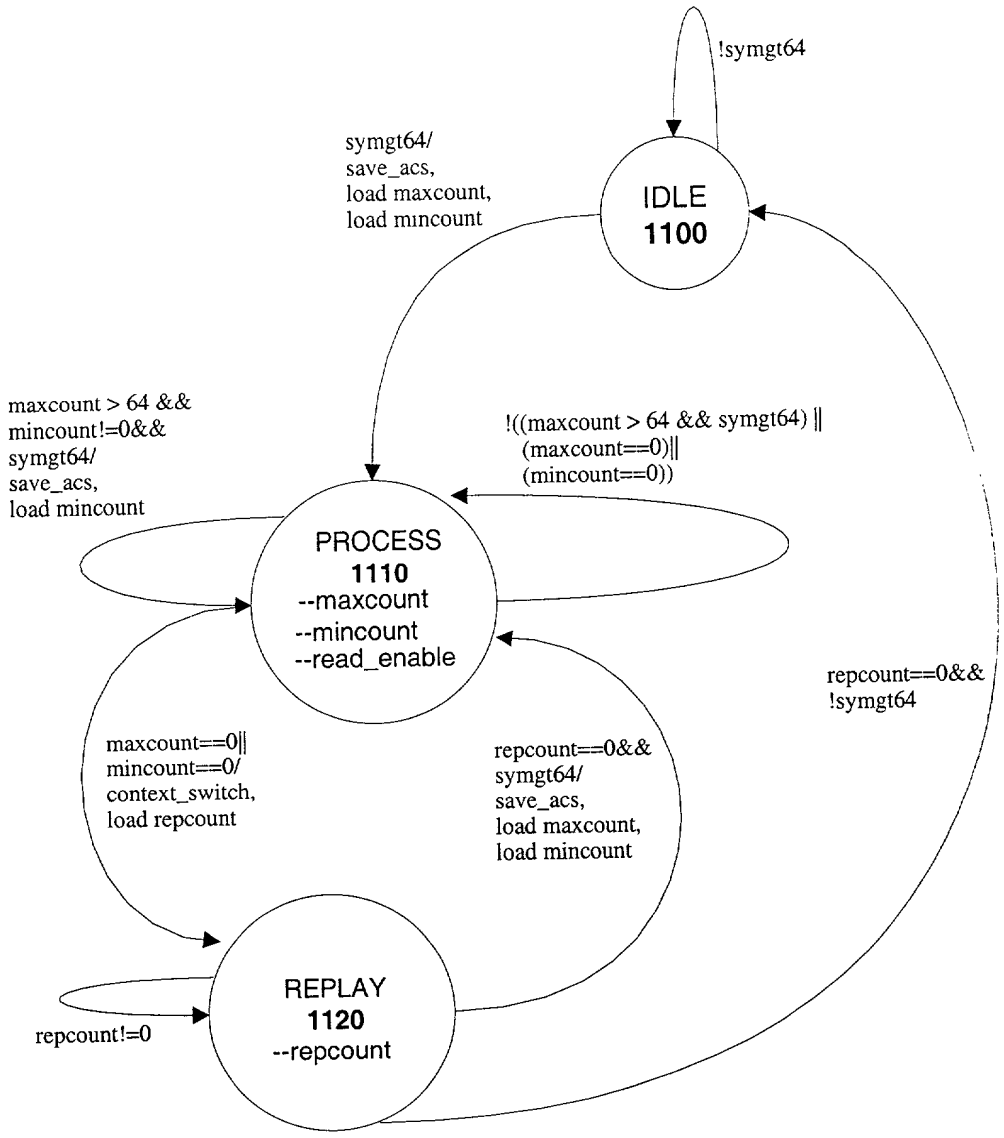
!symgt64
symgt64/
save_acs,
load maxcount,
load mincount
IDLE
1100
maxcount > 64 &&
mincount!=0&&
symgt64/
save_acs,
load mincount
!((maxcount > 64 && symgt64) ||
(maxcount==0)||
(mincount==0))
PROCESS
1110
--maxcount
--mincount
--read_enable
repcount==0&&
!symgt64
maxcount==0||
mincount==0/
context_switch,
load repcount
repcount==0&&
symgt64/
save_acs,
load maxcount,
load mincount
REPLAY
1120
--repcount
repcount!=0

Fig. 11

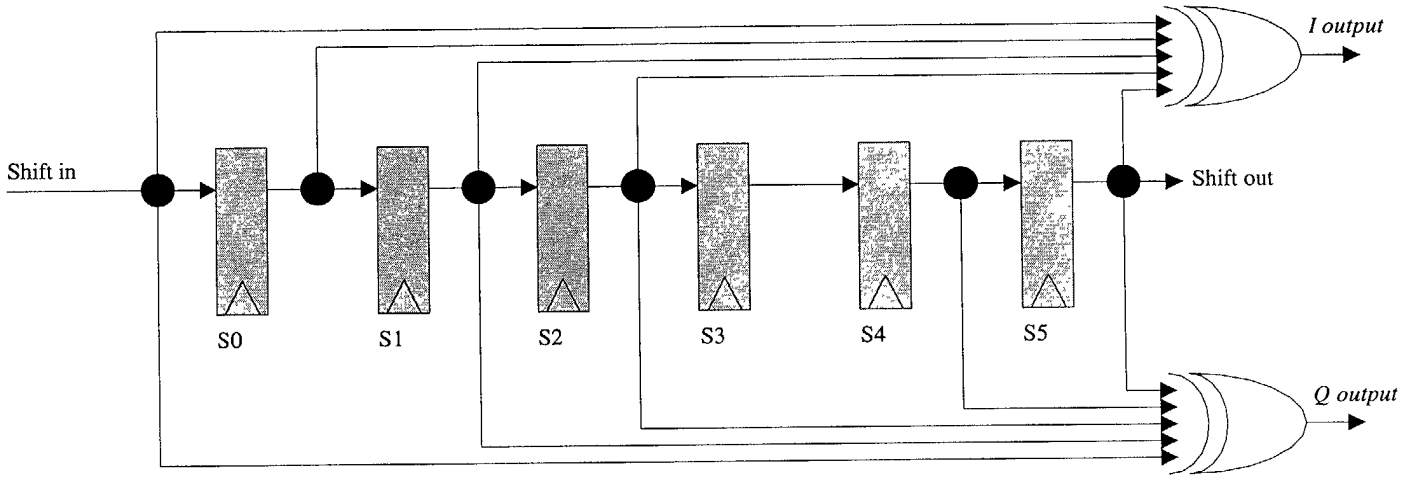

Fig. 12

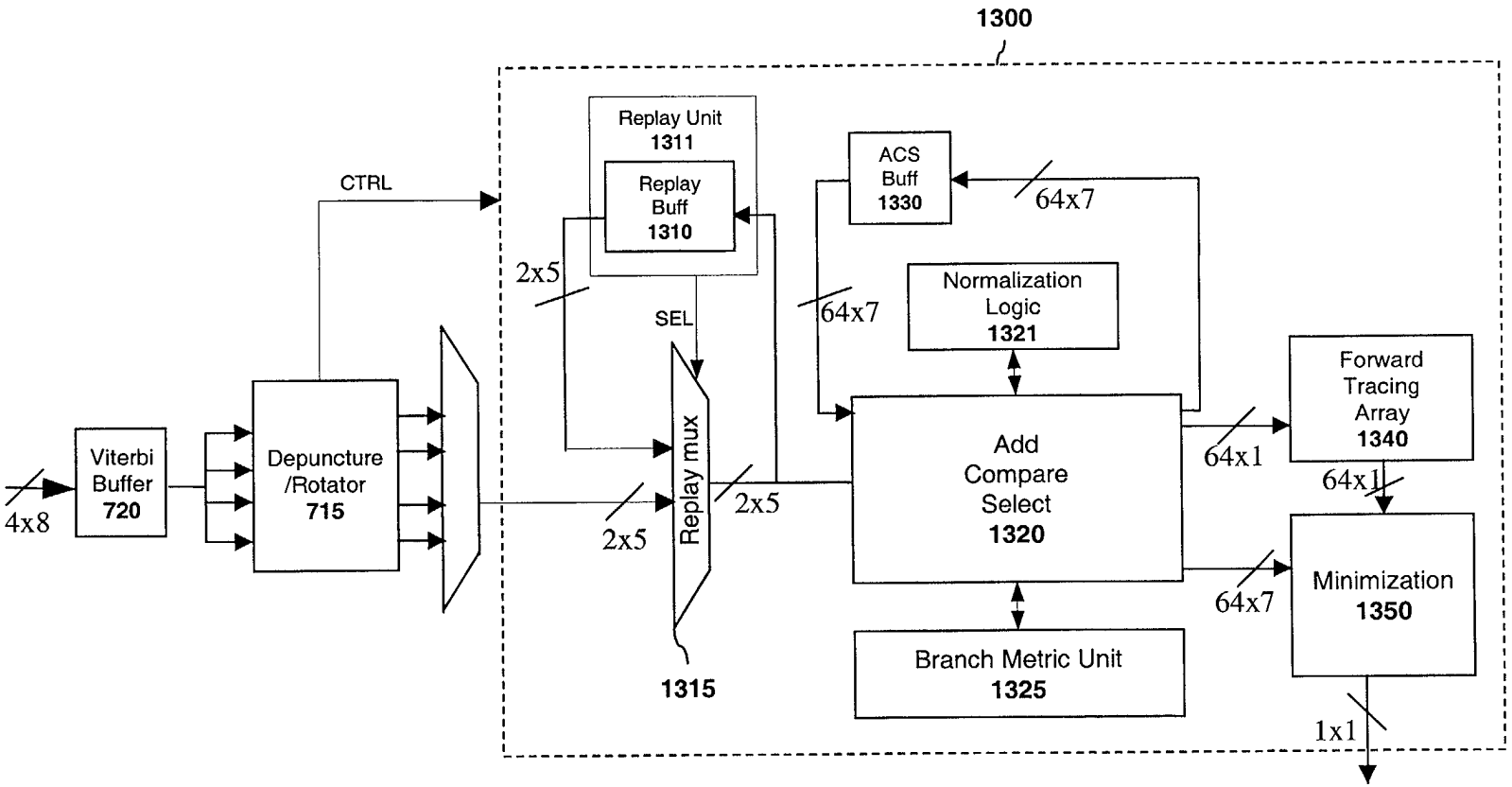

Fig. 13a

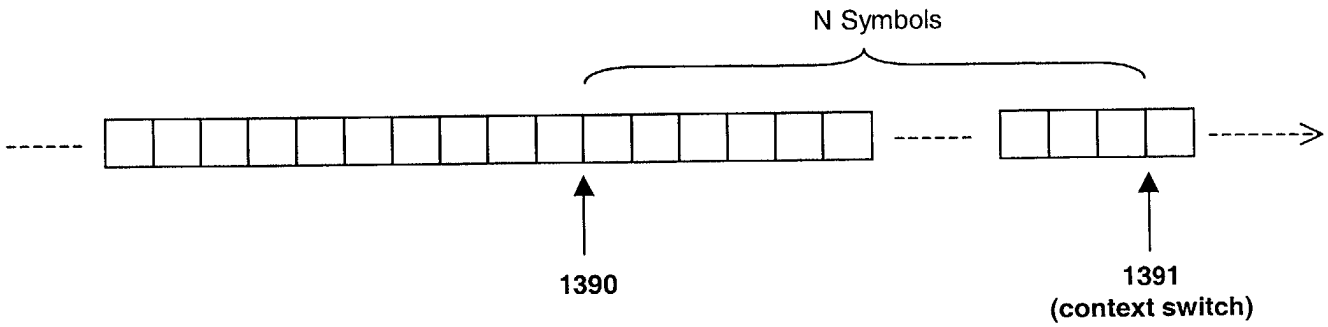

Fig. 13b

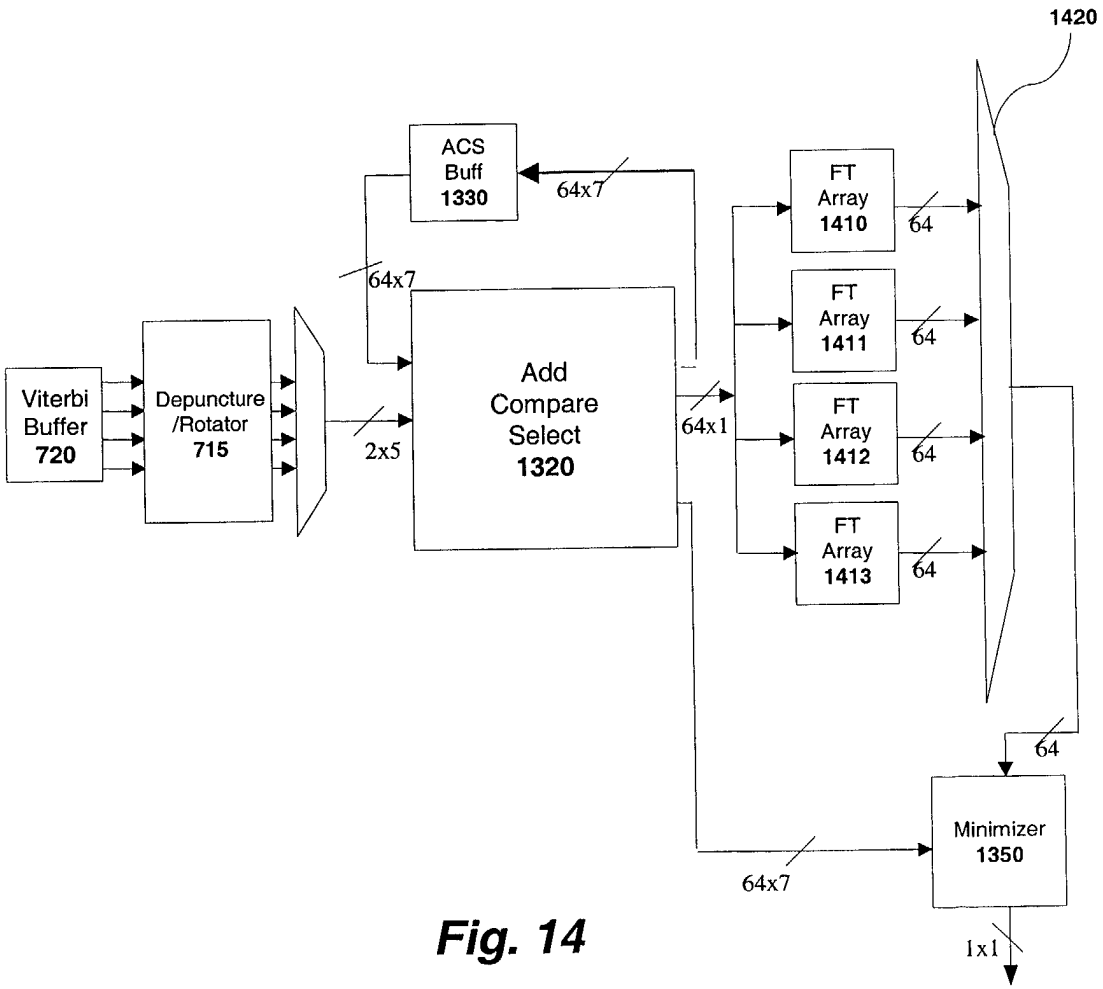
1420
ACS Buff 1330
64x7
FT Array 1410
64
64x7
FT Array 1411
64
Viterbi Buffer 720
Depuncture /Rotator 715
Add Compare Select 1320
2x5
64x1
FT Array 1412
64
FT Array 1413
64
64
Minimizer 1350
64x7
1x1

Fig. 14

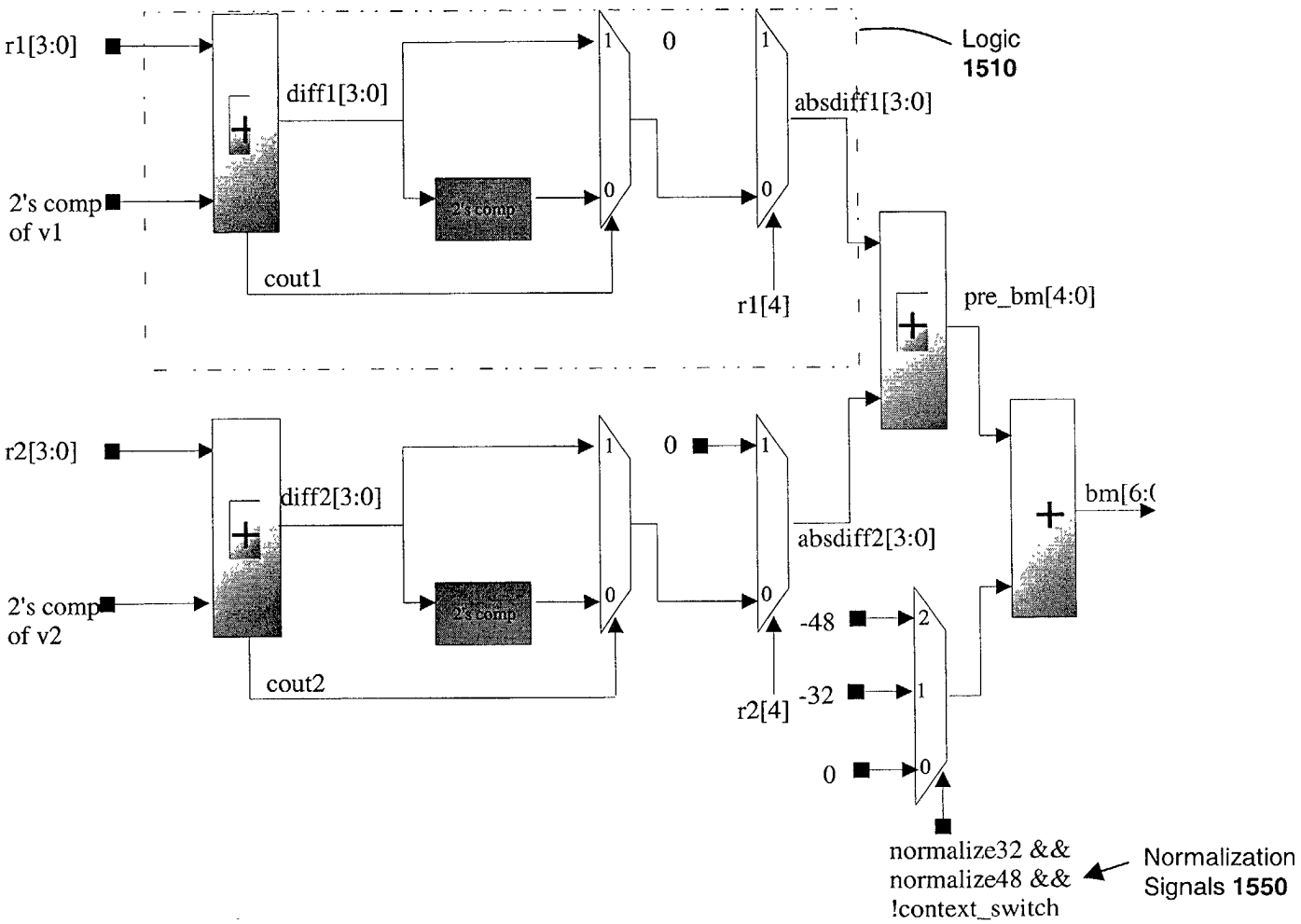
r1[3:0]
2's comp of v1
diff1[3:0]
cout1
2's comp
1
0
0
1
0
absdiff1[3:0]
r1[4]
Logic 1510
pre_bm[4:0]
r2[3:0]
2's comp of v2
diff2[3:0]
cout2
2's comp
1
0
0
1
0
absdiff2[3:0]
r2[4]
-48
-32
0
2
1
0
bm[6:0]
normalize32 &&
normalize48 &&
!context_switch
Normalization Signals 1550

Fig. 15

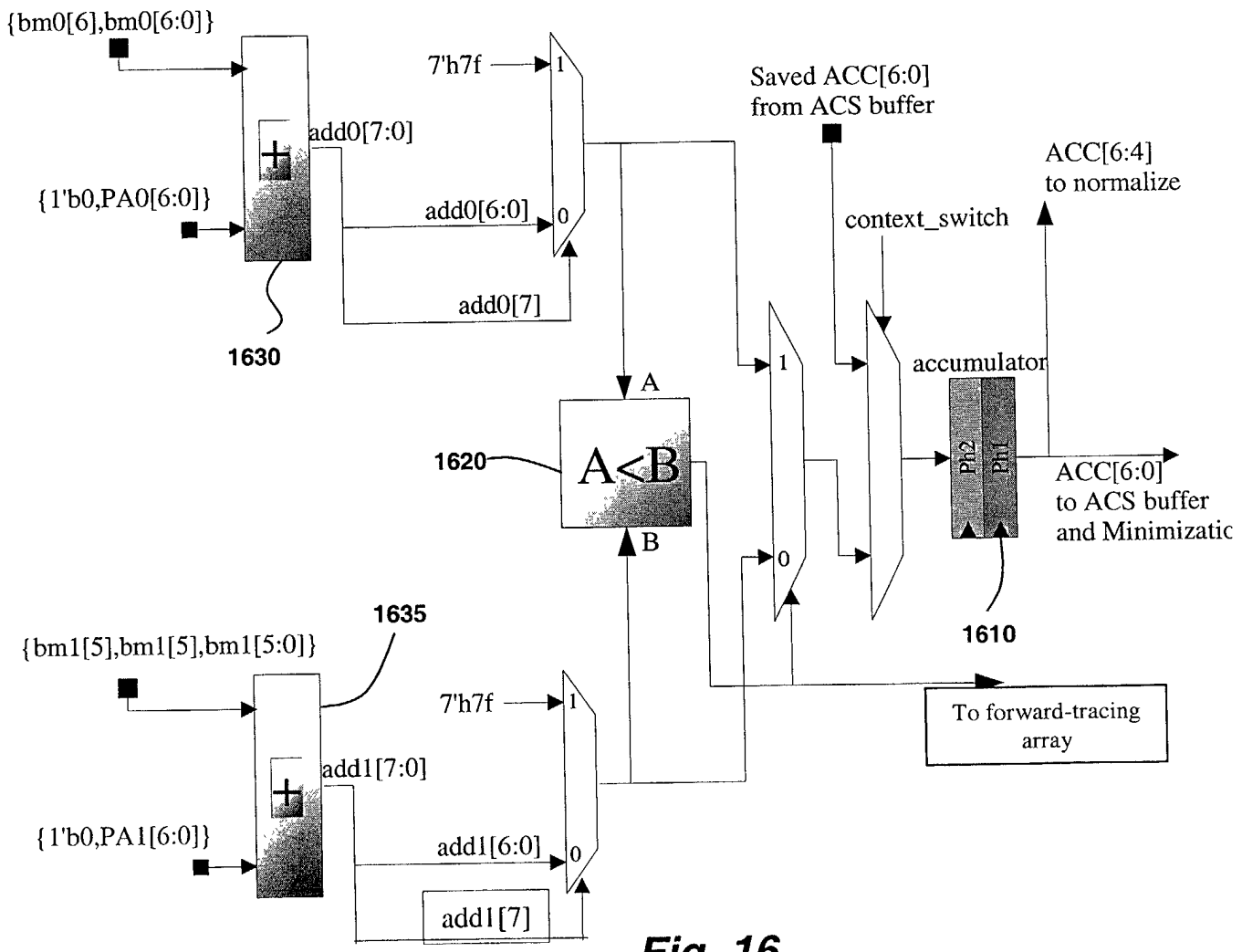
{bm0[6],bm0[6:0]}
7'h7f
1
add0[7:0]
Saved ACC[6:0]
from ACS buffer
ACC[6:4]
to normalize
{1'b0,PA0[6:0]}
add0[6:0]
0
context_switch
add0[7]
1630
accumulator
A
1620
A<B
1
Ph2
Ph1
ACC[6:0]
to ACS buffer
and Minimizatic
B
0
1635
1610
{bm1[5],bm1[5],bm1[5:0]}
7'h7f
1
To forward-tracing
array
add1[7:0]
{1'b0,PA1[6:0]}
add1[6:0]
0
add1[7]

Fig. 16

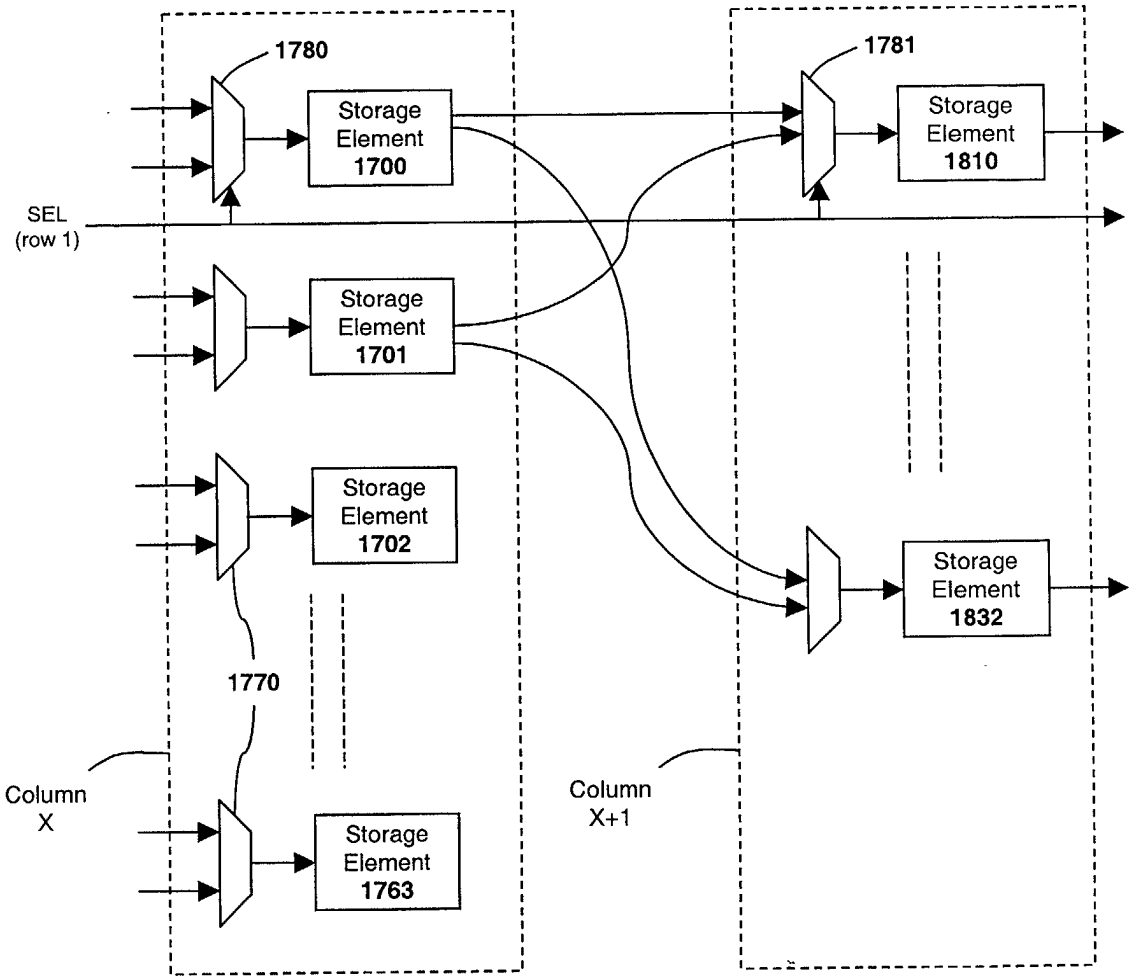

Fig. 17

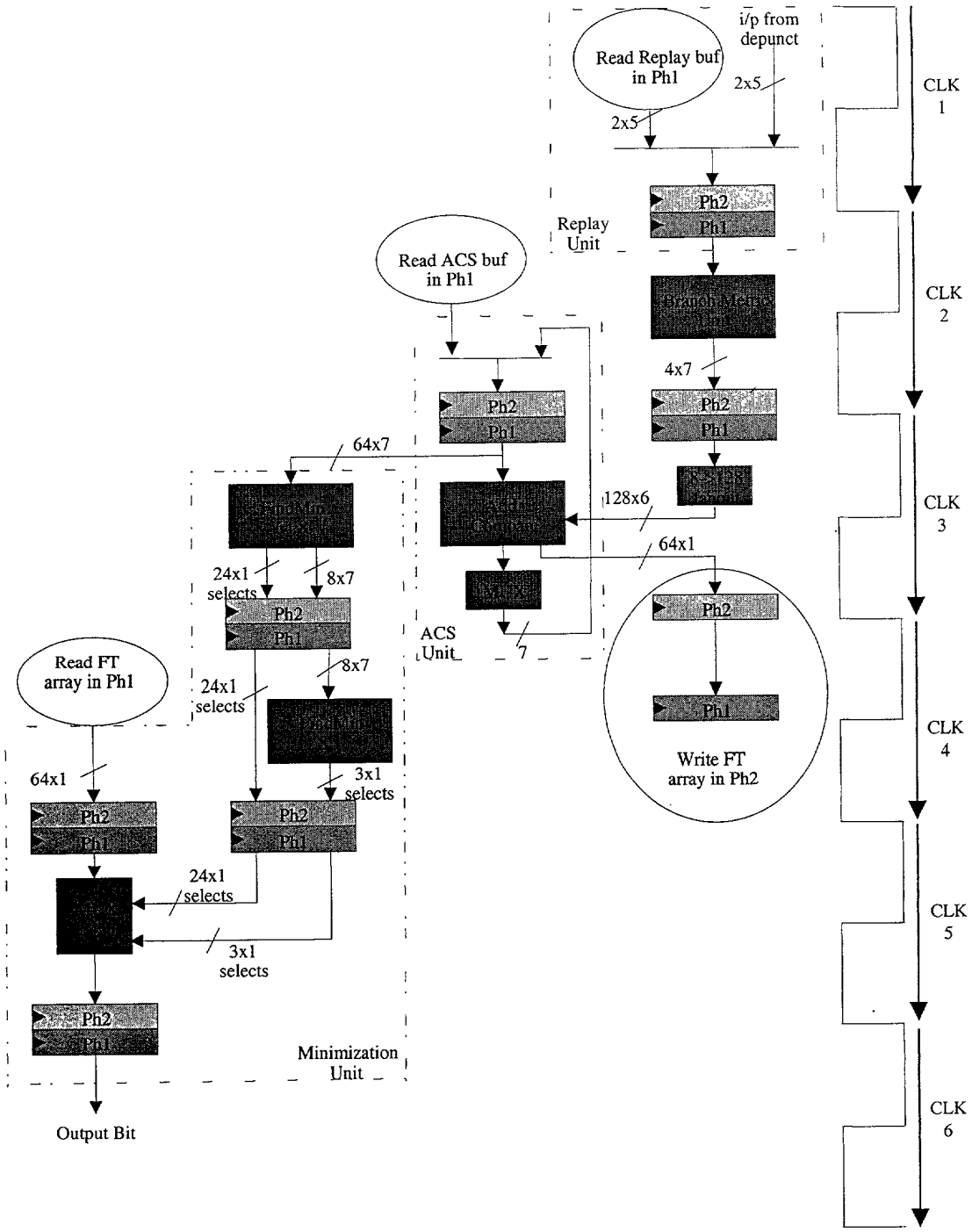
Read Replay buf in Ph1
i/p from depunct
2x5
2x5
CLK 1
Ph2
Ph1
Replay Unit
Read ACS buf in Ph1
CLK 2
4x7
Ph2
Ph1
64x7
128x6
CLK 3
64x1
24x1 selects
8x7
Ph2
Ph1
ACS Unit
7
Read FT array in Ph1
8x7
24x1 selects
64x1
3x1 selects
Ph2
Ph1
Write FT array in Ph2
CLK 4
24x1 selects
3x1 selects
CLK 5
Minimization Unit
Output Bit
CLK 6

Fig. 18

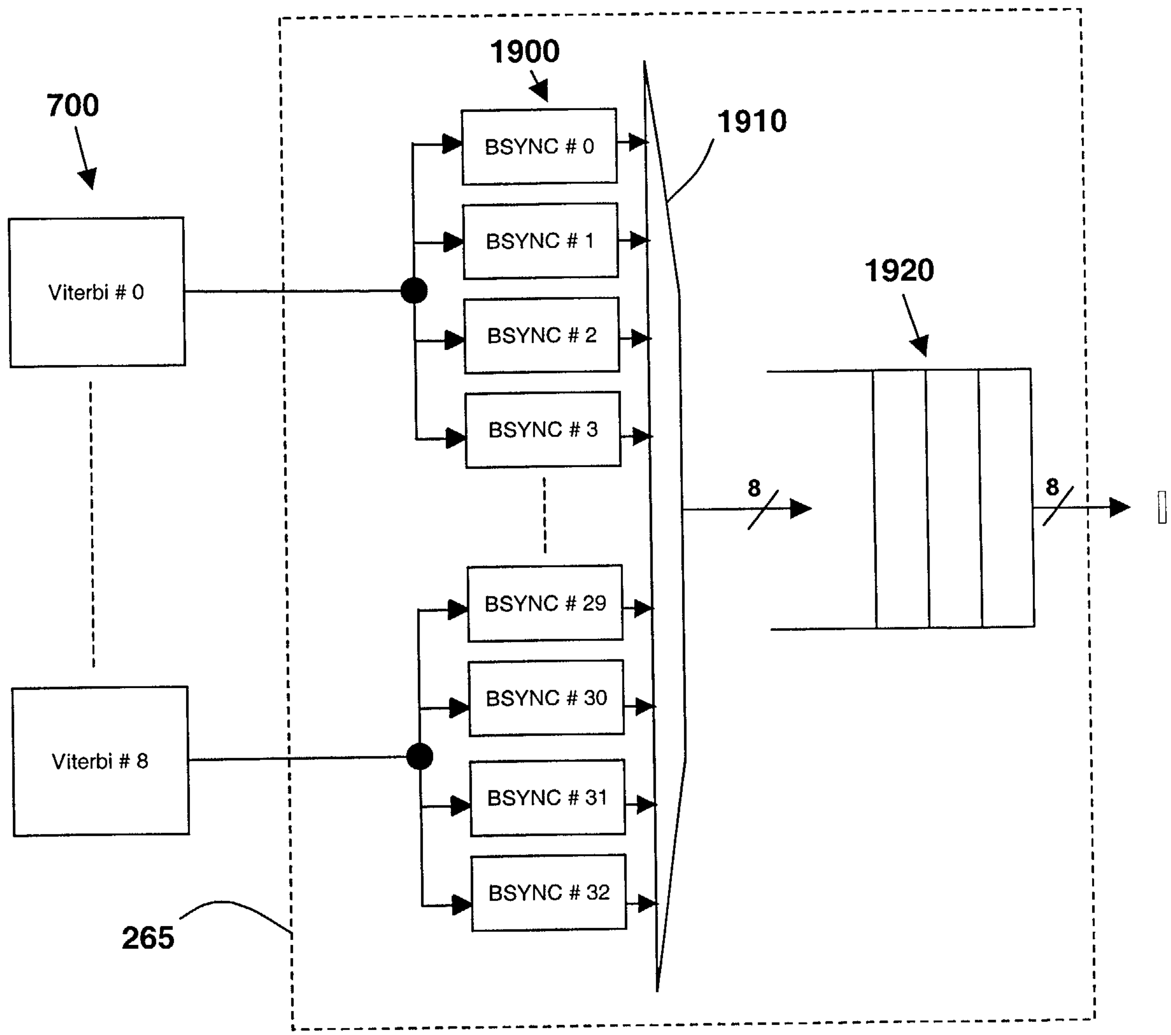
700
Viterbi # 0
Viterbi # 8
1900
BSYNC # 0
BSYNC # 1
BSYNC # 2
BSYNC # 3
BSYNC # 29
BSYNC # 30
BSYNC # 31
BSYNC # 32
1910
1920
8
8
265

Fig. 19

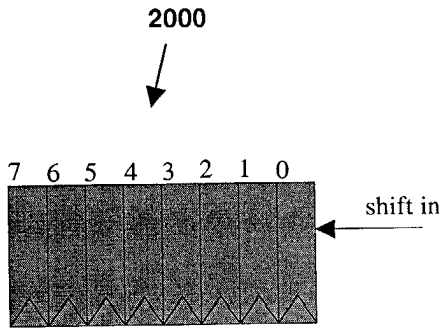

Fig. 20

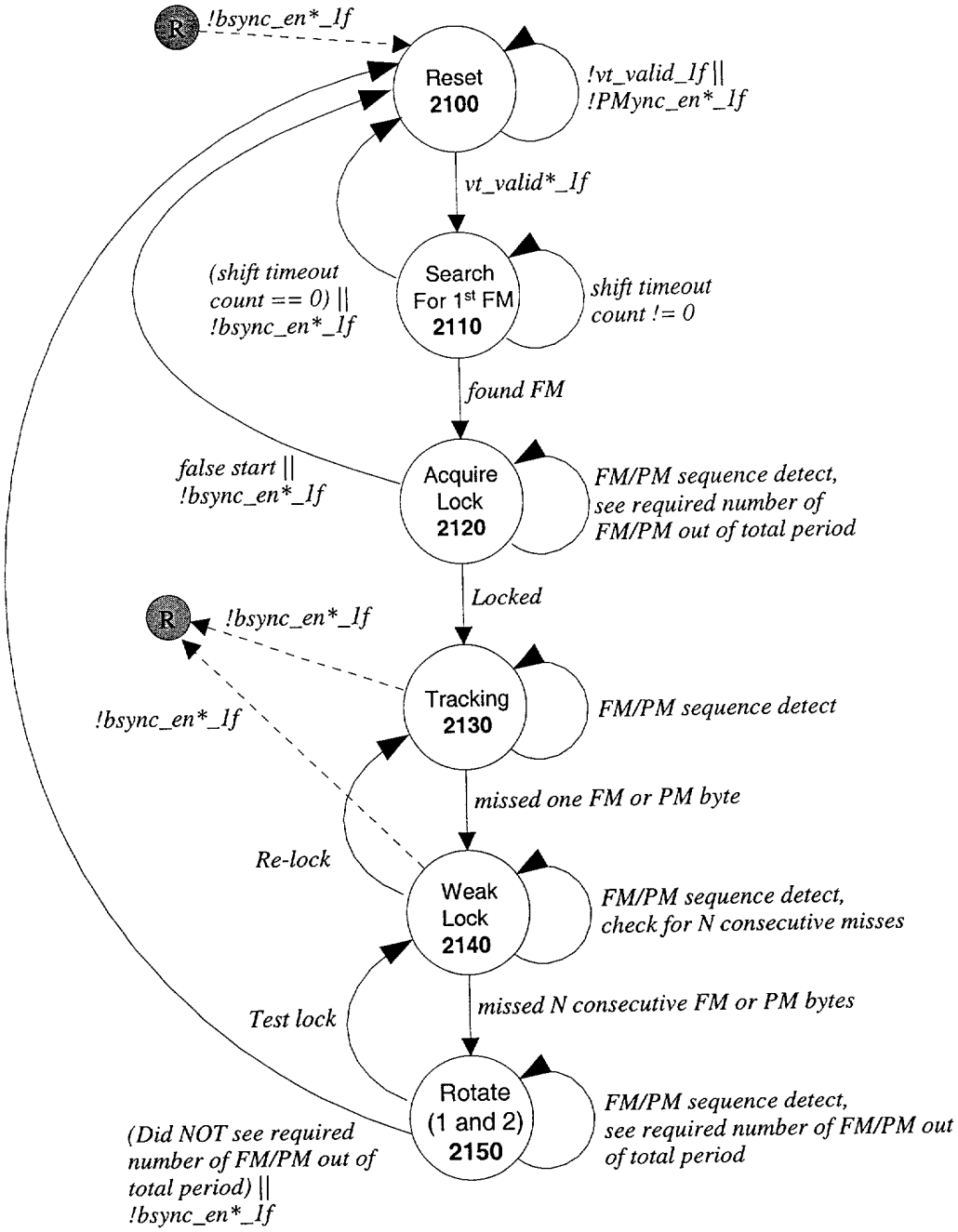
R
!bsync_en*_1f
Reset
2100
!vt_valid_1f ||
!PMync_en*_1f
vt_valid*_1f
(shift timeout
count == 0) ||
!bsync_en*_1f
Search
For 1st FM
2110
shift timeout
count != 0
found FM
false start ||
!bsync_en*_1f
Acquire
Lock
2120
FM/PM sequence detect,
see required number of
FM/PM out of total period
Locked
R
!bsync_en*_1f
!bsync_en*_1f
Tracking
2130
FM/PM sequence detect
missed one FM or PM byte
Re-lock
Weak
Lock
2140
FM/PM sequence detect,
check for N consecutive misses
missed N consecutive FM or PM bytes
Test lock
Rotate
(1 and 2)
2150
FM/PM sequence detect,
see required number of FM/PM out
of total period
(Did NOT see required
number of FM/PM out of
total period) ||
!bsync_en*_1f

Fig. 21

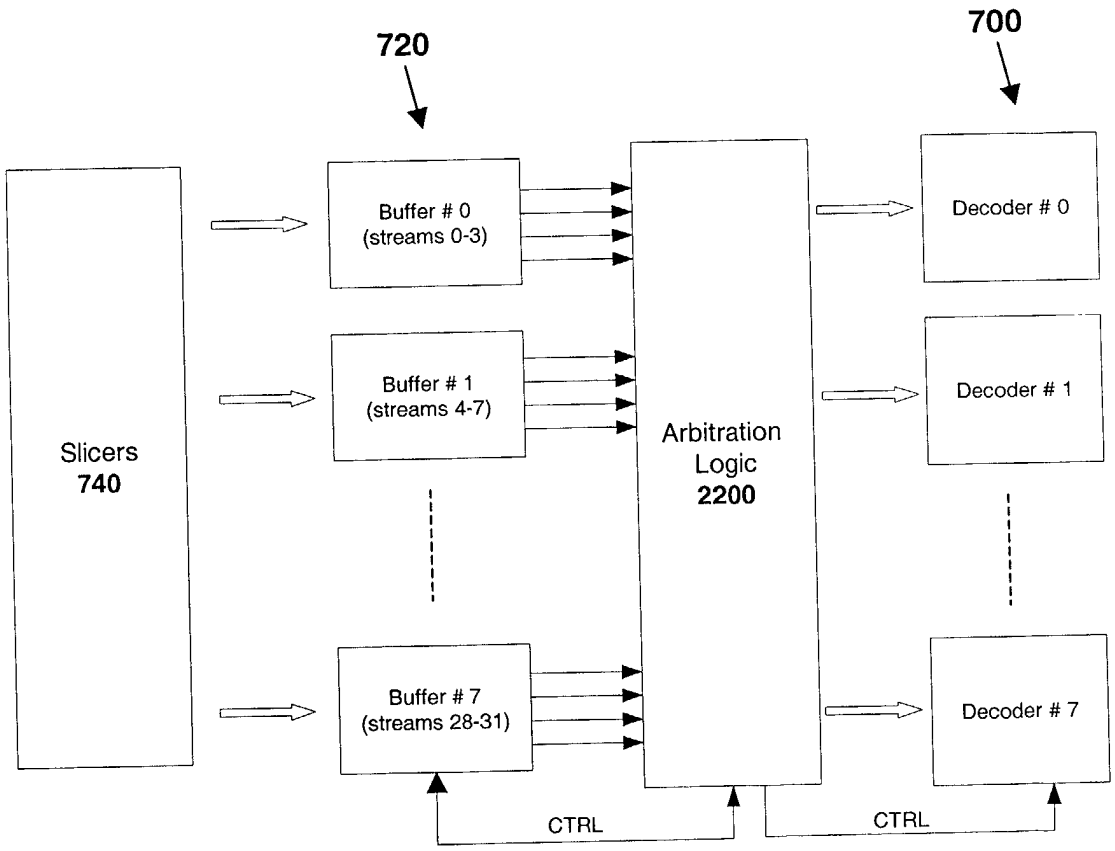
720
700
Slicers
740
Buffer # 0
(streams 0-3)
Buffer # 1
(streams 4-7)
Buffer # 7
(streams 28-31)
Arbitration
Logic
2200
Decoder # 0
Decoder # 1
Decoder # 7
CTRL
CTRL

Fig. 22

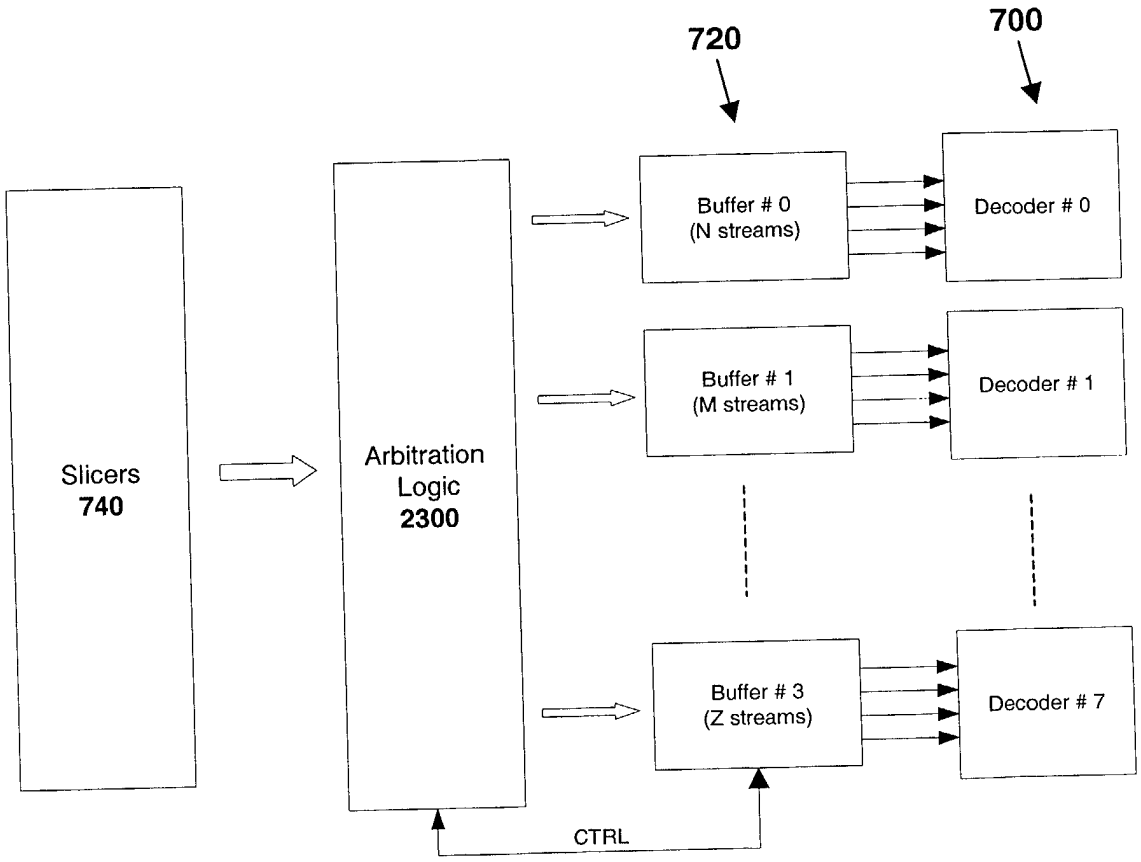
720
700
Slicers
740
Arbitration
Logic
2300
Buffer # 0
(N streams)
Buffer # 1
(M streams)
Buffer # 3
(Z streams)
Decoder # 0
Decoder # 1
Decoder # 7
CTRL

Fig. 23

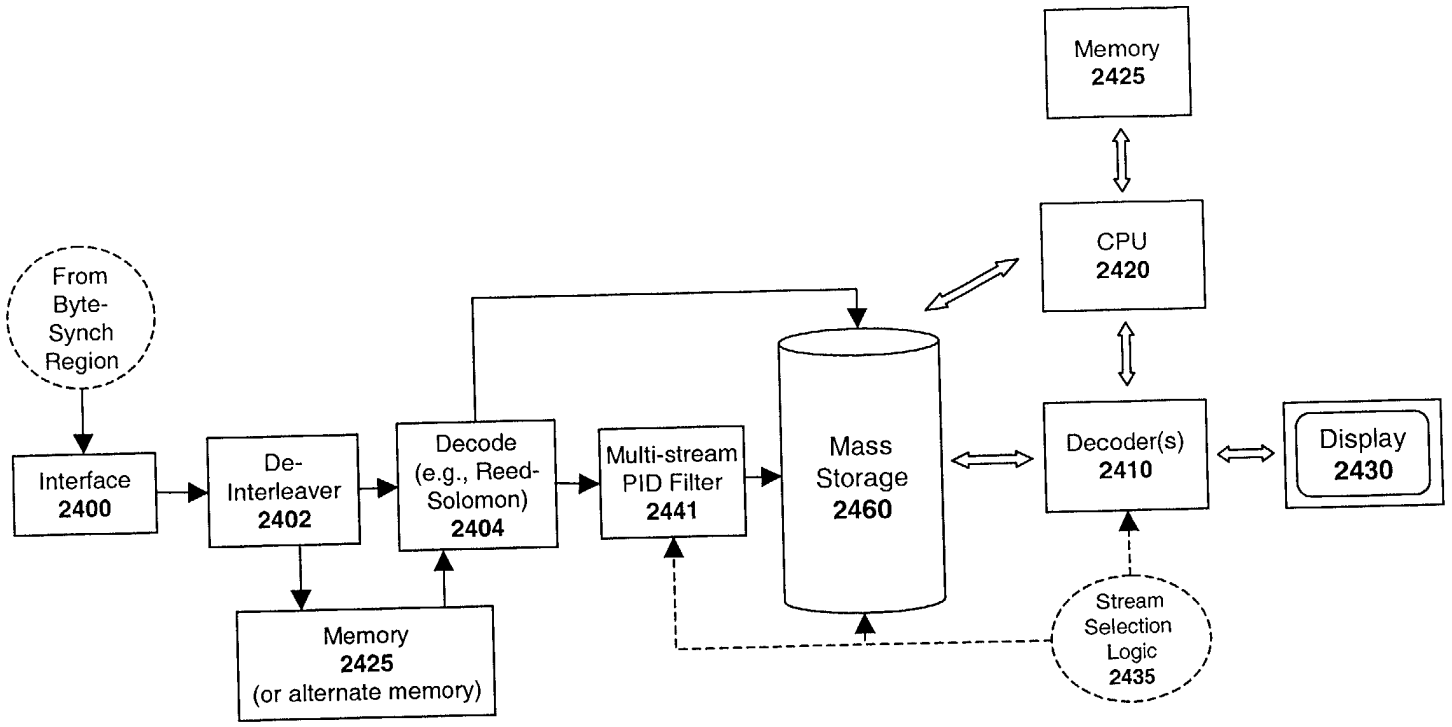
From Byte-Synch Region
Interface 2400
De-Interleaver 2402
Decode (e.g., Reed-Solomon) 2404
Memory 2425 (or alternate memory)
Multi-stream PID Filter 2441
Mass Storage 2460
Memory 2425
CPU 2420
Decoder(s) 2410
Display 2430
Stream Selection Logic 2435

Fig. 24